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The world owes Phillips and Signetics a great debt in introducing the SO package. It offers a very small footprint, low cost, reliable, surface mounting package demanded by today's high density systems. However, since the thermal impedance of any package is, to the first order, inversely proportional to its area, the SO-8 imposes severe restrictions on the allowable power dissipation of the package. As pointed out in Reference (1), power dissipation raises the die junction temperature, and system reliability may be degraded. This brief sets forth a practical design method to ascertain what, if any, restrictions have to be placed on operating a linear IC in the SO package.

Analysis

Probably the best place to begin is to establish at what junction temperature a given device will be allowed to operate. Most manufacturers rate their junctions at a maximum of 150°C in plastic packages, but for reasons of reliability, a lower number may be mandated. The datasheet usually stipulates θ_{JA}, the thermal impedance from junction to ambient, and the difference between the maximum junction temperature we will allow and the maximum ambient temperature stipulates the thermal budget that we have or the junction temperature rise:

$$Pt = \frac{T_J(max) - T_A(max)}{\theta_{JA}} \qquad \text{(EQ. 1)}$$

where:

Pt = Total Power Dissipated by the Device

T_J(max) = Maximum Junction Temperature

T_A(max) = Maximum Ambient Temperature

Power dissipation is comprised of two parts—Pq, the power dissipated by the device due simply to its supply current, and P_L, the power dissipated by the chip as a consequence of driving a load. In general, Pq is independent of P_L and vice versa, so an analysis can be made of each case and the results simply added together to obtain Pt.

The analysis should start with Pq since it is straightforward, and if T_J(max) is exceeded under quiescent conditions, an alternate strategy is dictated. A word of caution, however, is in order. There are devices such as the EL2001 Unity Gain Buffer that draw a supply current of 1mA but are capable of driving 100mA loads. Clearly, in this case, power dissipation will be dominated by P_L. As a case in point, we might examine the EL2120 100MHz CFA. Its quiescent supply current is specified as 20mA. A typical video application is to use ±10V power supplies with 150Ω load driven to 8V peak-to-peak with an ambient temperature of 50°C. Under these conditions, Pq is equal to 400mW, and using the datasheet value of l75°C/W for θ_{JA}, we obtain an average value for T_J of 120°C. What this tells us is that in order to keep the junction below 150°C, the junction rise due to driving a load must be under 30°C.

If we assume a steady state (sinusoidal) output voltage of 4V, the power dissipated in the EL2021's output transistor, P_L, would be:

$$P_L = (V+ - V_{OUT})(I_{OUT}) \qquad \text{(EQ. 2)}$$

Where:

$$I_{OUT} = \frac{V_{OUT}}{R_L'}$$

$$R_L' = R_L \parallel R_F$$

The recommended feedback resistor for the EL2120 is typically 300Ω, and for an inverter, R_F is indeed in parallel with R_L. For our particular case, P_L is equal to 240mW, and the additional increase in junction temperature is 42°C exceeding our earlier requirement of limiting the load incurred junction rise to less than 30°C and putting the junction at an average of 162°C.

In the final analysis, either the supply voltages have to be reduced or the load decreased to maintain the junction temperature below 150°C. Our best advice is to approach the problem carefully, do the Pq “spot check” first, and verify the conditions with the vendor's applications department.

References

1. “Reliability and the Electronic Engineer” by Barry Siegel, paper given at the EE Times Analog conference, October, 1991
2. “A Simple Method for Characterizing Hybrid Package Thermal Impedances” by Steve Ott and Barry Siegel, Hybrid Circuit Technology, June, 1990