

改善的業界標準單端電流模式 PWM 控制器

可調頻率、低電源、電流模式PWM控制器的系列：ISL6840, ISL6841, ISL6842、ISL6843、ISL6844和ISL6845是設計用于大範圍能量變換應用，包括升壓、反饋和隔離輸出的結構。峰值電流模式控制可有效地處理能量瞬變且有固有的過流保護。

這個先進的BiCMOS設計不但兼容了業界標準384x控制器系列的引腳，而且顯著地改善了其性能。其特點包括低運作電流、60A 啟動電流、可調工作頻率高達2MHz和20ns升降時間的高峰值電流驅動力。

零件號碼	上升欠壓切斷	最大占空比
ISL6840	7.0V	100%
ISL6841	7.0V	50%
ISL6842	14.4V	100%
ISL6843	8.4V	100%
ISL6844	14.4V	50%
ISL6845	8.4V	50%

主要特點

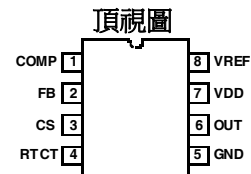
- 1A MOSFET 驅動器
- 60 μ A 啟動電流, 其峰值為 100 μ A
- 控制到輸出的延遲是 30ns
- 高峰值電流模式控制固有的快速瞬變反應
- 可調開關頻率高達 2MHz
- 20ns 升降時間以 1nF 輸出負載
- 平衡的定時電容的放電電流適合于精確死區時間/最大占空比控制
- 高帶寬誤差放大器
- 遍及輸入、負載和溫度範圍的精密的容差電壓基準精密的容差電流門限值
- 不含 Pb 的包裝

應用

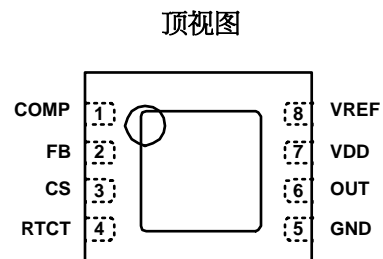
- 電信和信息電源
- 無線基站電源
- 檔案服務器電源
- 工業動力系統
- 個人計算機電源
- 隔離降壓和反饋變換器
- 升壓調節器

插腳引線

ISL6840, ISL6841, ISL6842, ISL6843, ISL6844, ISL6845
(8-PIN SOIC, MSOP)



(8-PIN DFN)



ISL6840, ISL6841, ISL6842, ISL6843, ISL6844, ISL6845

定購資料

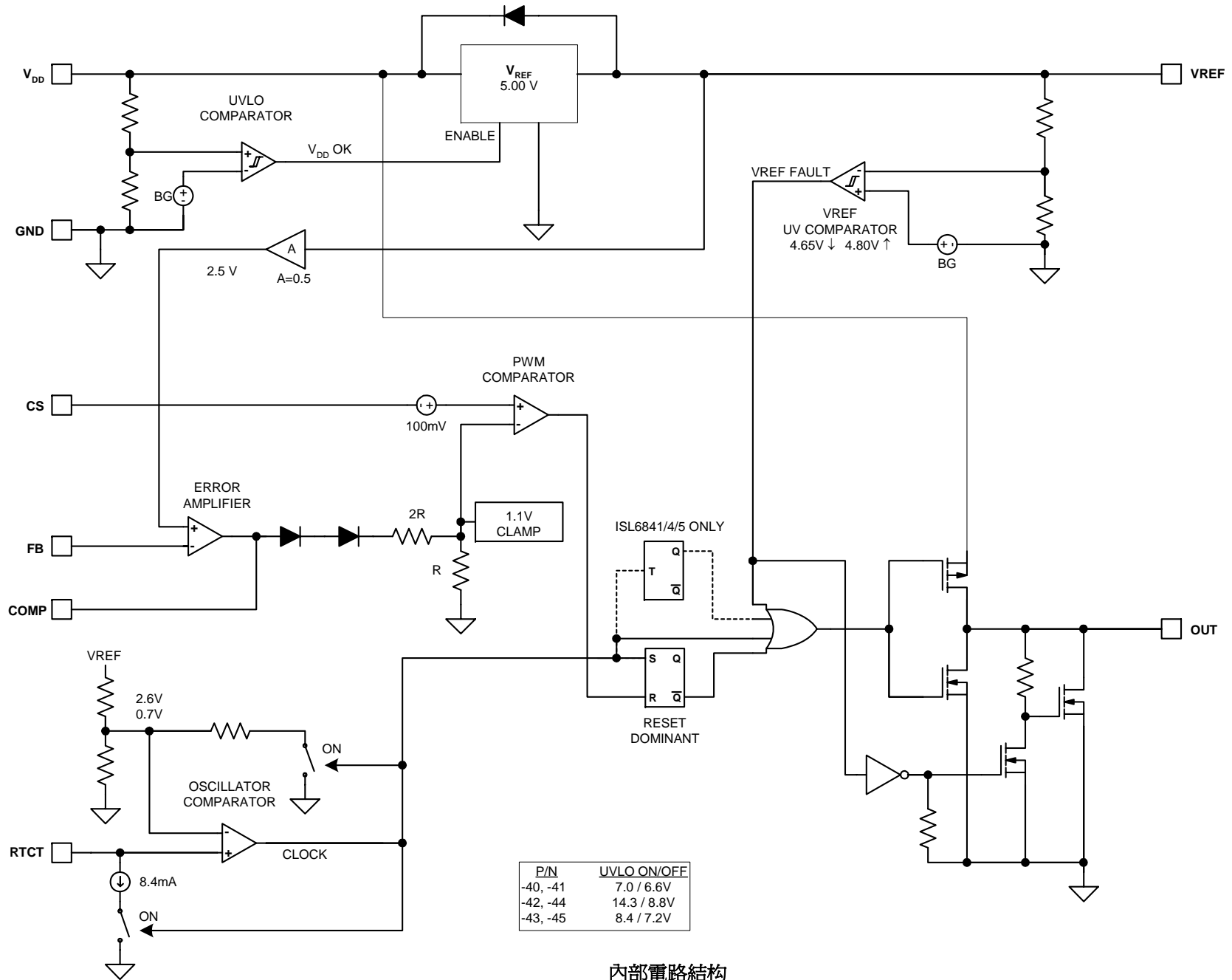
零件號碼	溫度範圍 (°C)	包裝	包裝圖號 #
ISL6840IB	-40 to 105	8 Ld SOIC	M8.15
ISL6840IBZ (See Note)	-40 to 105	8 Ld SOIC (Pb-free)	M8.15
ISL6840IU	-40 to 105	8 Ld MSOP	M8.118
ISL6840IUZ (See Note)	-40 to 105	8 Ld MSOP (Pb-free)	M8.118
ISL6841IB	-40 to 105	8 Ld SOIC	M8.15
ISL6841IBZ (See Note)	-40 to 105	8 Ld SOIC (Pb-free)	M8.15
ISL6841IU	-40 to 105	8 Ld MSOP	M8.118
ISL6841IUZ (See Note)	-40 to 105	8 Ld MSOP (Pb-free)	M8.118
ISL6842IB	-40 to 105	8 Ld SOIC	M8.15
ISL6842IBZ (See Note)	-40 to 105	8 Ld SOIC (Pb-free)	M8.15
ISL6842IU	-40 to 105	8 Ld MSOP	M8.118
ISL6842IUZ (See Note)	-40 to 105	8 Ld MSOP (Pb-free)	M8.118
ISL6843IB	-40 to 105	8 Ld SOIC	M8.15
ISL6843IBZ (See Note)	-40 to 105	8 Ld SOIC (Pb-free)	M8.15
ISL6843IU	-40 to 105	8 Ld MSOP	M8.118
ISL6843IUZ (See Note)	-40 to 105	8 Ld MSOP (Pb-free)	M8.118
ISL6844IB	-40 to 105	8 Ld SOIC	M8.15
ISL6844IBZ (See Note)	-40 to 105	8 Ld SOIC (Pb-free)	M8.15
ISL6844IU	-40 to 105	8 Ld MSOP	M8.118
ISL6844IUZ (See Note)	-40 to 105	8 Ld MSOP (Pb-free)	M8.118
ISL6845IB	-40 to 105	8 Ld SOIC	M8.15
ISL6845IBZ (See Note)	-40 to 105	8 Ld SOIC (Pb-free)	M8.15
ISL6845IU	-40 to 105	8 Ld MSOP	M8.118
ISL6845IUZ (See Note)	-40 to 105	8 Ld MSOP (Pb-free)	M8.118
ISL6840IRZ-T* (See Note)	-40 to 105	8 Ld 2x3 DFN (Pb-free)	L8.2x3
ISL6841IRZ-T* (See Note)	-40 to 105	8 Ld 2x3 DFN (Pb-free)	L8.2x3
ISL6842IRZ-T (See Note)	-40 to 105	8 Ld 2x3 DFN (Pb-free)	L8.2x3
ISL6843IRZ-T (See Note)	-40 to 105	8 Ld 2x3 DFN (Pb-free)	L8.2x3

零件號碼	溫度範圍 (°C)	包裝	包裝圖號 #
ISL6844IRZ-T* (See Note)	-40 to 105	8 Ld 2x3 DFN (Pb-free)	L8.2x3
ISL6845IRZ-T (See Note)	-40 to 105	8 Ld 2x3 DFN (Pb-free)	L8.2x3

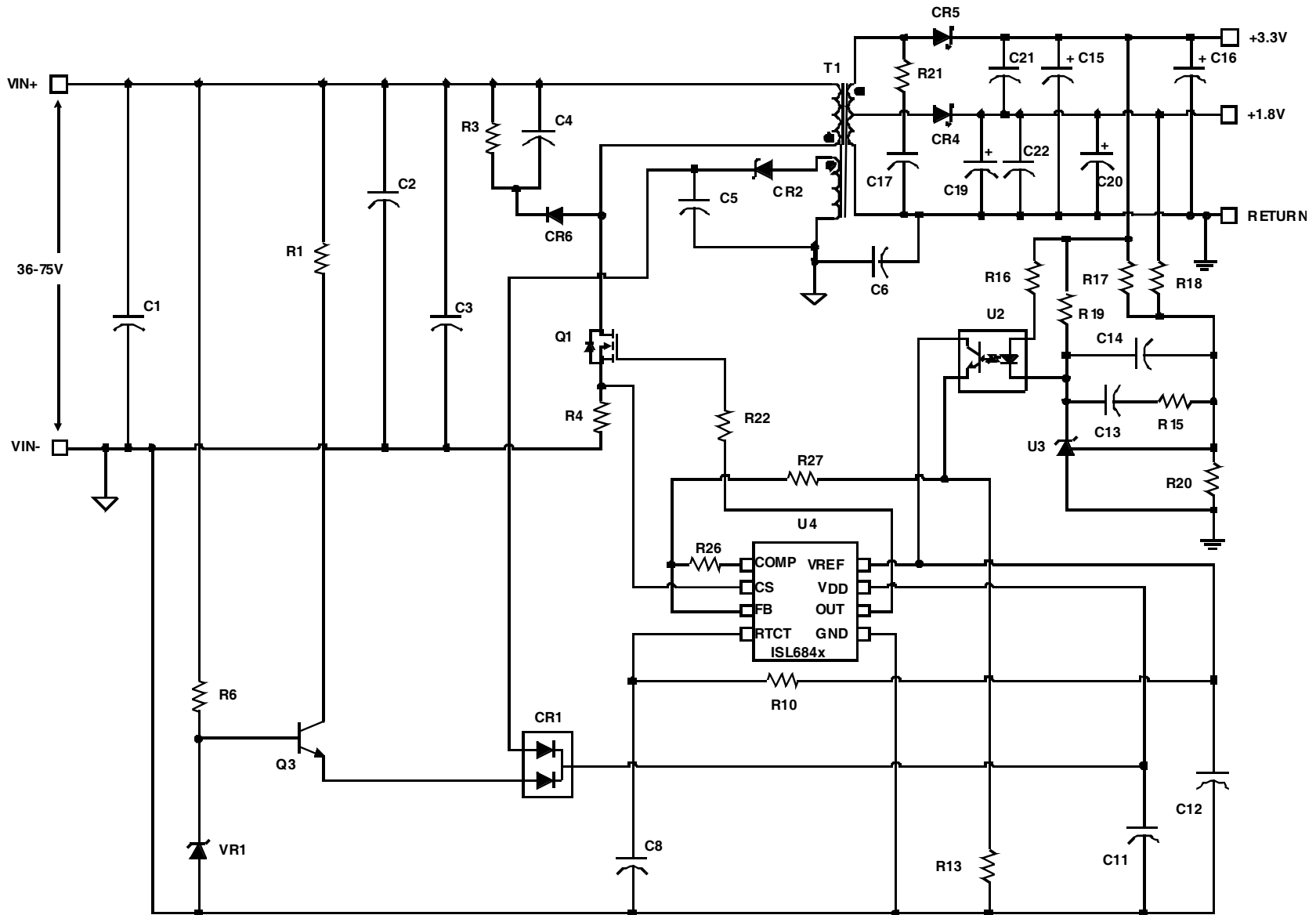
Add -T to part number for Tape and Reel packaging

*Contact Factory for Availability

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020



內部電路結構



典型應用: 48V 輸入雙輸出反饋轉換器

ISL6840, ISL6841, ISL6842, ISL6843, ISL6844, ISL6845

額定値

Supply Voltage, V_{DD}	-GND-0.3V to +20V
OUT	GND - 0.3V to $V_{DD} + 0.3V$
Signal Pins	GND-0.3V to 6.0V
Peak GATE Current	1A
ESD Classification	
Human Body Model (Per MIL-STD-883 Method 3015.7)	2000V
Charged Device Model (Per EOS/ESD DS5.3, 4/14/93)	1000V

運行條件

Supply Voltage Range (Typical)	
ISL6840/1	7.5V-14VDC
ISL6843/5	9-16VDC
ISL6842/4	15V-18VDC
Temperature Range	
ISL684xix	-40°C to 105°C

熱性能的資料

Thermal Resistance (Typical, Note 1) θ_{JA} (°C/W)	θ_{JC} (°C/W)
DFN Package (Note 2)	77
SOIC Package	100
MSOP Package	130
Maximum Junction Temperature	-55°C to 150°C
Maximum Storage Temperature Range	-65°C to 150°C
Maximum Lead Temperature (Soldering 10s) (SOIC – Lead Tips Only)	300°C

CAUTION: Stress above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied.

Notes:

- θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
- For θ_{JC} , the "case temp" location is the center of the exposed metal pad on the package underside.
- All voltages are to be measured with respect to GND, unless otherwise specified.

電気規範		Electrical Specifications			
Recommended Operating Conditions, Unless Otherwise Noted. Refer to Block Diagram and Typical Application Schematic.					
$V_{DD} = 15V$ (Note 7), $R_T = 10K\Omega$, $C_T = 3.3nF$, $T_A = -40^\circ C$ to $105^\circ C$ (Note 4), Typical values are at $T_A = 25^\circ C$.					
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
UNDERVOLTAGE LOCKOUT					
START Threshold (ISL6840, ISL6841)		6.5	7.0	7.5	V
START Threshold (ISL6843, ISL6845)		7.8	8.4	9.0	V
START Threshold (ISL6842, ISL6844)		13.3	14.3	15.3	V
STOP Threshold (ISL6840, ISL6841)		6.1	6.6	6.9	V
STOP Threshold (ISL6843, ISL6845)		6.7	7.2	7.7	
STOP Threshold (ISL6842, ISL6844)		8.0	8.8	9.6	V
Hysteresis (ISL6840, ISL6841)		-	0.4	-	V
Hysteresis (ISL6843, ISL6845)		-	0.8	-	V
Hysteresis (ISL6842, ISL6844)		-	5.4	-	V
Start-Up Current, I_{DD}	$V_{DD} < \text{START Threshold}$	-	60	100	μA
Operating Current, I_{DD}	(Note 5)	-	3.3	4.0	mA
Operating Supply Current, I_D	Includes 1nF GATE loading	-	4.1	-	mA
REFERENCE VOLTAGE					
Overall Accuracy	Over line ($V_{DD} = 12V$ to $18V$), load, temp	4.925	5.000	5.050	V
Long Term Stability	$T_A = 125^\circ C$, 1000 hours (Note 6)	-	5	-	mV
Fault Voltage		4.40	4.65	4.85	V
VREF Good Voltage		4.60	4.80	VREF-0.05	V
Hysteresis		50	165	250	mV
Current Limit, Sourcing		-20	-	-	mA

ISL6840, ISL6841, ISL6842, ISL6843, ISL6844, ISL6845

Current Limit, Sinking		5	-	-	mA
Electrical Specifications					
电气规范 Recommended Operating Conditions, Unless Otherwise Noted. Refer to Block Diagram and Typical Application Schematic. $V_{DD} = 15V$ (Note 6), $R_T = 10K\Omega$, $C_T = 3.3nF$, $T_A = -40^\circ C$ to $105^\circ C$ (Note 3), Typical values are at $T_A = 25^\circ C$. (continued)					
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
CURRENT SENSE					
Input Bias Current	$V_{CS} = 1V$	-1.0	-	1	μA
CS Offset Voltage	$V_{CS} = 0V$ (Note 6)	95	100	105	mV
COMP to PWM Comparator Offset Voltage	$V_{CS} = 0V$ (Note 6)	0.80	1.15	1.30	V
Input Signal, Maximum		0.91	0.97	1.03	V
Gain, $A_{CS} = DV_{COMP}/DV_{CS}$	$0 < V_{CS} < 910mV$, $V_{FB} = 0V$ (Note 6)	2.5	3	3.5	V/V
CS to OUT Delay	(Note 6)	-	25	40	nS
ERROR AMPLIFIER					
Open Loop Voltage Gain	(Note 6)	60	90	-	dB
Unity Gain Bandwidth	(Note 6)	3.5	5	-	MHz
Reference Voltage	$V_{FB} = V_{COMP}$	2.475	2.500	2.525	V
FB Input Bias Current	$V_{FB} = 0$	-1.0	-0.2	1.0	μA
COMP Sink Current	$V_{COMP} = 1.5V$, $V_{FB} = 2.7V$	1.0	-	-	mA
COMP Source Current	$V_{COMP} = 1.5V$, $V_{FB} = 2.3V$	-0.4	-	-	mA
COMP VOH	$V_{FB} = 2.3V$	4.80	-	VREF	V
COMP VOL	$V_{FB} = 2.7V$	0.4	-	1.0	V
PSRR	Frequency = 120Hz, $V_{DD} = 12V$ to $18V$ (Note 6)	60	80	-	dB
OSCILLATOR					
Frequency Accuracy	Initial, $T_J = 25^\circ C$	49	52	55	KHz
Frequency Variation with V_{DD}	$T = 25^\circ C$ ($F_{18V} - F_{12V}$)/ F_{12V}	-	0.2	1.0	%
Temperature Stability	(Note 6)	-	-	5	%
Amplitude, Peak to Peak		-	1.9	-	V
RTCT Discharge Voltage		-	0.7	-	V
Discharge Current	RTCT = 2.0V	7.2	8.4	9.5	mA
OUTPUT					
Gate VOH	$V_{DD} - OUT$, $I_{OUT} = -200mA$	-	1.0	2.0	V
Gate VOL	OUT - GND, $I_{OUT} = 200mA$	-	1.0	2.0	V
Peak Output Current	$C_{OUT} = 1nF$ (Note 6)	-	1.0	-	A
Rise Time	$C_{OUT} = 1nF$ (Note 6)	-	20	40	nS
Fall Time	$C_{OUT} = 1nF$ (Note 6)	-	20	40	nS
PWM					
Maximum Duty Cycle	ISL6840, ISL6842, ISL6843	94	96	-	%
	ISL6841, ISL6844, ISL6845	47	48	-	%

ISL6840, ISL6841, ISL6842, ISL6843, ISL6844, ISL6845

Electrical Specifications

电气规范

Recommended Operating Conditions, Unless Otherwise Noted. Refer to Block Diagram and Typical Application Schematic.

$V_{DD} = 15V$ (Note 6), $R_T = 10K\Omega$, $C_T = 3.3nF$, $T_A = -40^\circ C$ to $105^\circ C$ (Note 3), Typical values are at $T_A = 25^\circ C$. (continued)

Minimum Duty Cycle	ISL6840, ISL6842, ISL6843	-	-	0	%
	ISL6841, ISL6844, ISL6845	-	-	0	%

Notes:

- Specifications at $-40^\circ C$ are guaranteed by design, not production tested.
- This is the V_{DD} current consumed when the device is active but not switching. Does not include gate drive current.
- Guaranteed by design, not 100% tested in production.
- Adjust V_{DD} above the start threshold and then lower to 15V.

典型性能曲線圖

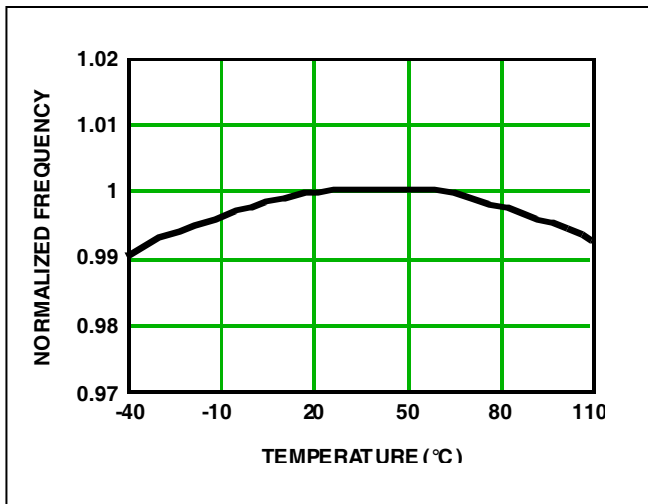


FIGURE 1. FREQUENCY vs TEMPERATURE

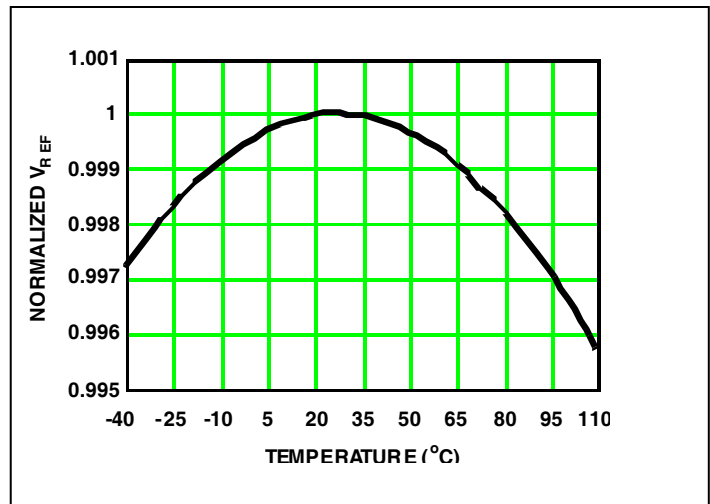


FIGURE 2. REFERENCE VOLTAGE vs TEMPERATURE

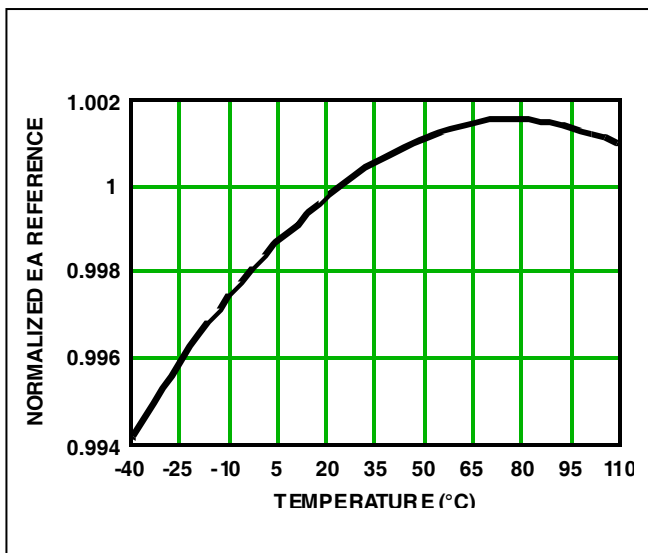


FIGURE 3. EA REFERENCE vs TEMPERATURE

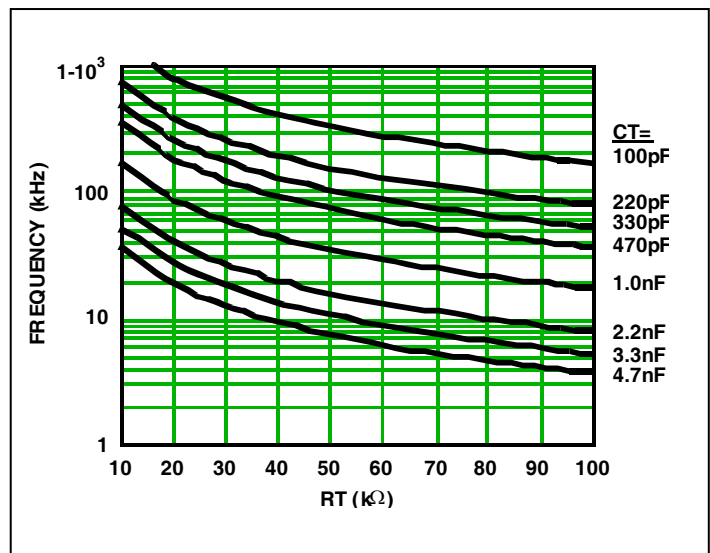


FIGURE 4. RTCT vs FREQUENCY

各管腳簡介

RTCT

這是振蕩器定時控制引腳。由這引腳間連接一電阻(RT)到 VREF 与和一定時電容(CT)到 GND 之間可設置工作頻率和最大占空比。振蕩器產生一個可調頻率高達 2.0MHz 的鋸齒波。充電時間 (TC)、放電時間 (TD)、開關頻率 (f) 和最大占空比 (Dmax) 可用以下等式計算:

$$T_C \approx 0.583 \cdot R_T \cdot C_T \quad (\text{EQ. 1})$$

$$T_D \approx -R_T \cdot C_T \cdot \ln\left(\frac{0.0083 \cdot R_T - 4.3}{0.0083 \cdot R_T - 2.4}\right) \quad (\text{EQ. 2})$$

$$f = 1/(T_C + T_D) \quad (\text{EQ. 3})$$

$$D_{\max} = T_C \cdot f \quad (\text{EQ. 4})$$

在選擇電容和電阻值所需指定的頻率時，可用圖4作為指南。

COMP

COMP是誤差放大器的輸出端和PWM比較器的輸入端。控制環頻率補償網絡應連接在COMP 和FB引腳之間。

FB

通過這個引腳輸出電壓的反饋連接到誤差放大器的倒相輸入，而誤差放大器的正相輸入連接于內部的基準電壓。

CS

這是PWM 比較器電流檢測輸入端。輸入信號的範圍在典型值0到1.0V，且有100mV 內部偏壓。

GND

器件上所有功能和電源地都以這個引腳為基準。

OUT

這是電源開關元件的驅動輸出端。它具有 1.0A 峰值電流驅動 MOSFET 門極。當 VDD 低于 UVLO 門限值時，門極輸出就會降低。

VDD

VDD是電源輸入端。總供應電流取決于OUT輸出負載，而總IDD電流是工作電流和平均輸出電流之和。平均輸出電流與工作頻率 (f) 和MOSFET門極電荷 (Qg) 成正比，可用以下公式計算：

$$I_{\text{OUT}} = Q_g \cdot f \quad (\text{EQ. 5})$$

要優化抗擾度，用一個陶瓷電容器盡可能靠近并跨接在 V_{DD} 和 GND 引腳。

VREF

這是5.00V的基準電壓輸出端，且有+1.0/-1.5%的容差遍及輸入、負載和溫度範圍。可連接0.1μF至3.3μF的電容至GND以作濾波這輸出所需。

功能概述

主要特點

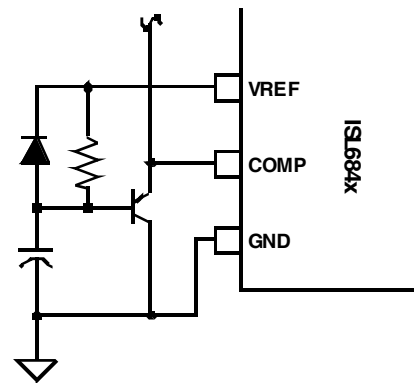
ISL684x 電流模式PWMs 為那些低成本反激式和正激式拓撲結構的應用提供了一個理想的選擇。因為其改善性能的遠勝過于業界標準零件，所以ISL684x是新設計或更新現存設計的優先選擇。

振蕩器

ISL684x控制器有一個可調頻率高達2MHz的鋸齒振蕩器。在 RTCT引腳連接一電阻至VREF和電容至 GND可設置工作頻率。(電阻和電容所需的指定頻率可參見圖4。)

軟啟動運作

軟啟動必須在外部實施。以一方法為例 說明如下,電壓鉗位在 COMP。



SOFT START

FIGURE 5. SOFT START

門極驅動器

ISL684x 可灌出和吸收 1A 峰值電流。要限制峰值電流通過 IC，可放置一個外部電阻在 IC 的推拉輸出(OUT 引腳)和 MOSFET 門極之間。而這個小串聯電阻能阻尼由線組寄生電感和 FET 的輸入電容的共振所產生的振蕩。

斜坡補償

應用的最大占空比少于 50%時，斜坡補償可提高抗擾度，尤其在負載較小時。測試表明：要優化抗擾度則需用一定數量的斜坡補償，一般約是 10% 全方位的電流反饋信號。若應用的占空比大于 50% 時，則需用斜坡補償來防止不穩定，而所需的最低量斜坡補償是相當于電感下坡的一半。外加過量的斜坡補償，會導致控制環路由電流模式控制轉化為電壓模式控制。

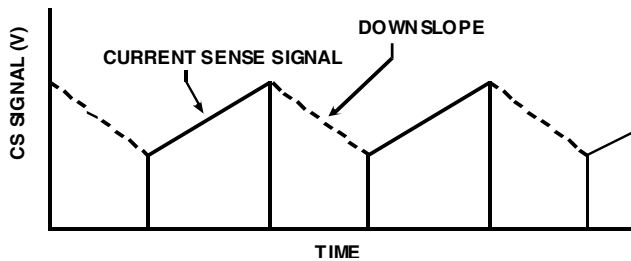


FIGURE 6. CURRENT SENSE DOWNSLOPE

用以下方式可增加傾斜補償的 CS 信號

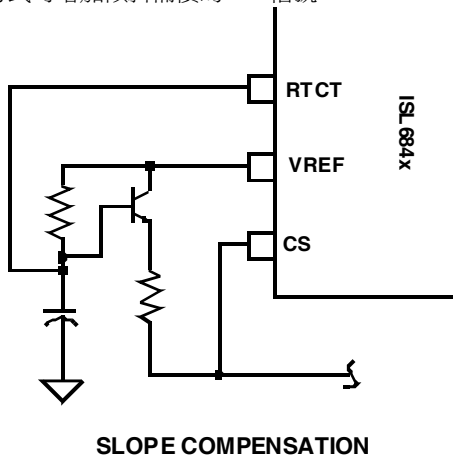


FIGURE 7. SLOPE COMPENSATION

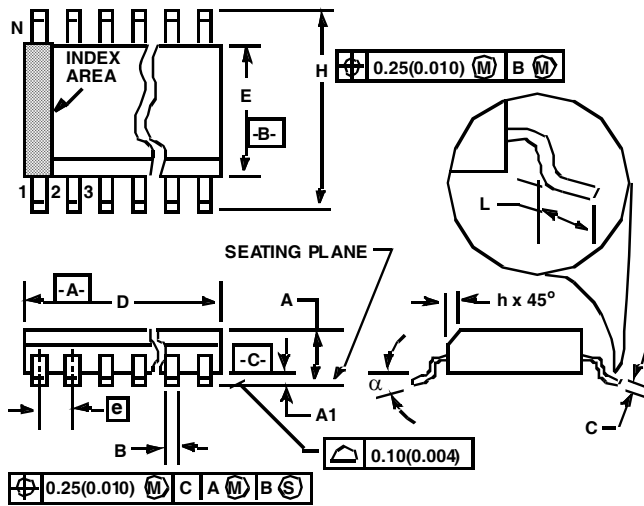
故障保護

VREF 跌落低于4.65V時會產生故障。當檢測出故障時，OUT 輸出就會被截止。VREF 超過4.80V時，則排除了故障，且OUT 會重新輸出。

接地面

為這個器件能理想操作，應要仔細布局，特別是應用一個好的接地面。其中獨一部分的接地面必須設置為高的DI/DT 電流輸出，且VDD 必須以一個好的高頻電容直接連接到地(GND)。

Small Outline Plastic Packages (SOIC)



M8.15 (JEDEC MS-012-AA ISSUE C)
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

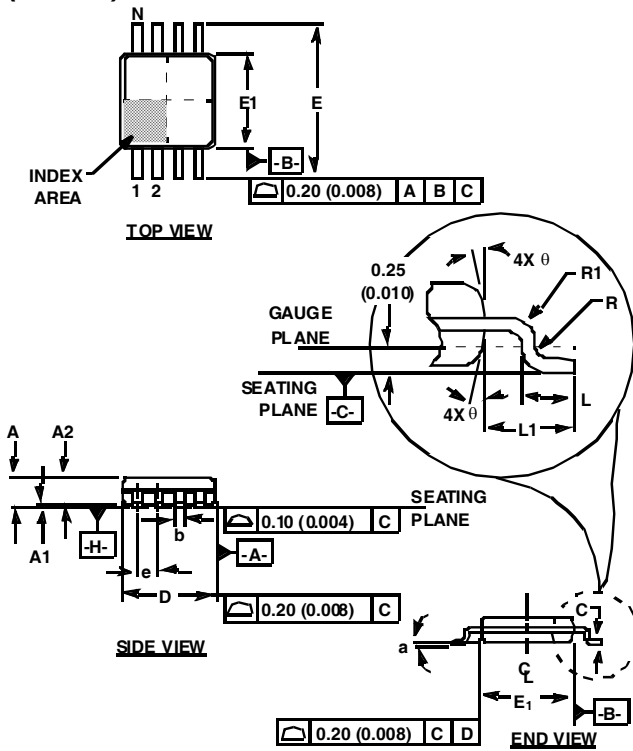
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
alpha	0°	8°	0°	8°	-

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs and are measured at Datum Plane. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions and are measured at Datum Plane. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are for reference only

Rev.0 12/93

**Mini Small Outline Plastic Packages
(MSOP)**



Notes:

1. These package dimensions are within allowable dimensions of JEDEC MO-187BA.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.
3. Dimension "D" does not include mold flash, protrusions or gate burrs and are measured at Datum Plane. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E1" does not include interlead flash or protrusions and are measured at Datum Plane. Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. Formed leads shall be planar with respect to one another within 0.10mm (0.004) at seating Plane.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of "b" dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Datums -A- and -B- to be determined at Datum plane -H-.
11. Controlling dimension: MILLIMETER. Converted inch dimensions are for reference only.

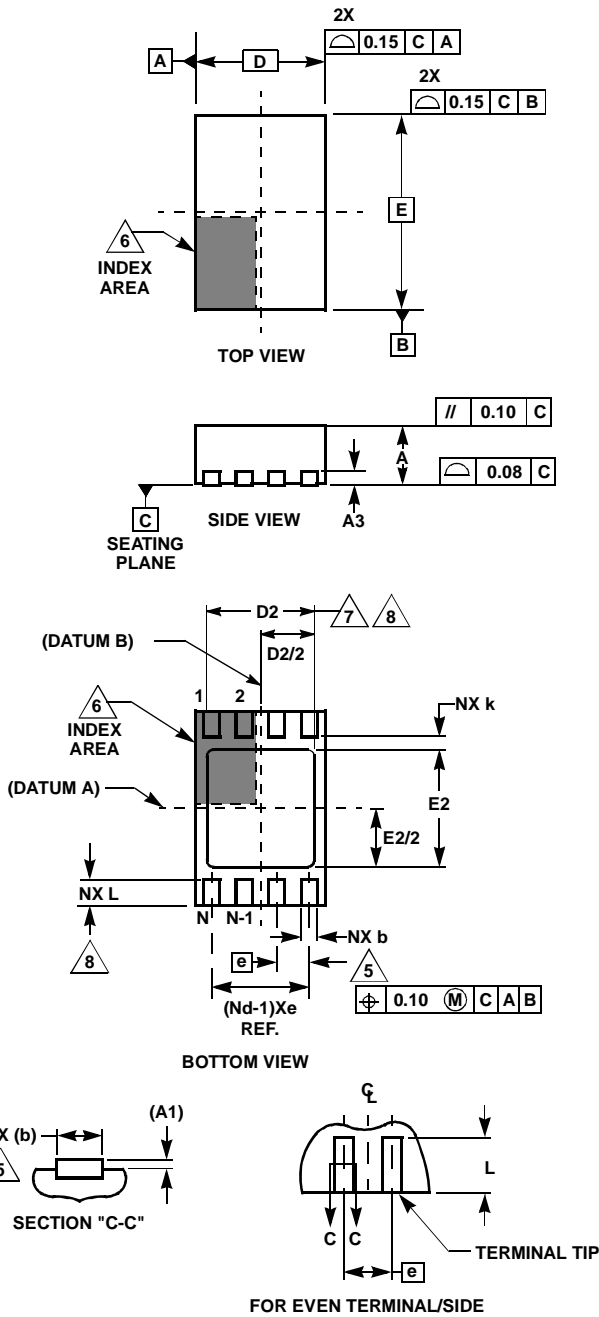
M8.118 (JEDEC MO-187AA)

8 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.037	0.043	0.94	1.10	-
A1	0.002	0.006	0.05	0.15	-
A2	0.030	0.037	0.75	0.95	-
b	0.010	0.014	0.25	0.36	9
c	0.004	0.008	0.09	0.20	-
D	0.116	0.120	2.95	3.05	3
E1	0.116	0.120	2.95	3.05	4
e	0.026 BSC		0.65 BSC		-
E	0.187	0.199	4.75	5.05	-
L	0.016	0.028	0.40	0.70	6
L1	0.037 REF		0.95 REF		-
N	8		8		7
R	0.003	-	0.07	-	-
R1	0.003	-	0.07	-	-
θ	5°	15°	5°	15°	-
α	0°	6°	0°	6°	-

Rev.2 01/03

Dual Flat No-Lead Plastic Package (DFN)



L8.2x3

8 LEAD DUAL FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A3	0.20 REF			-
b	0.20	0.25	0.32	5,8
D	2.00 BSC			-
D2	1.50	1.65	1.75	7,8
E	3.00 BSC			-
E2	1.65	1.80	1.90	7,8
e	0.50 BSC			-
k	0.20	-	-	-
L	0.30	0.40	0.50	8
N	8			2
Nd	4			3

Rev. 0 6/04

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd refers to the number of terminals on D.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.25mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.

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