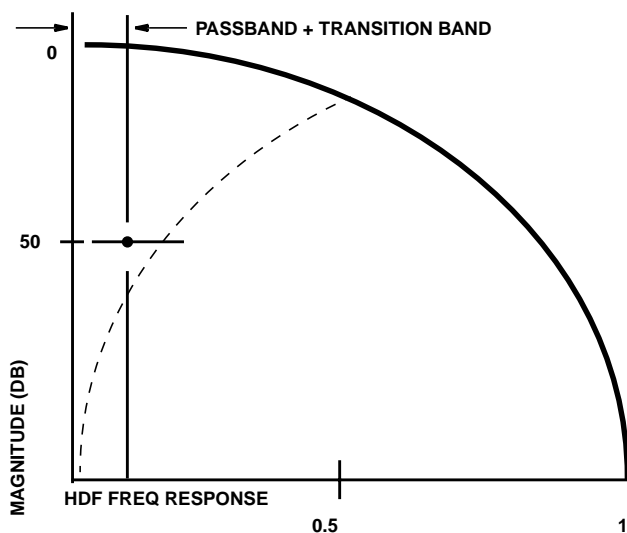


In order to maximize effectiveness of DECIMATE software there are two design rule checks that need some in depth discussion. Once these crosschecks are understood the usefulness of DECIMATE and the DDF will improve because filters that were previously thought unrealizable are in fact achievable. Consider the following normalized HDF response (to first null).

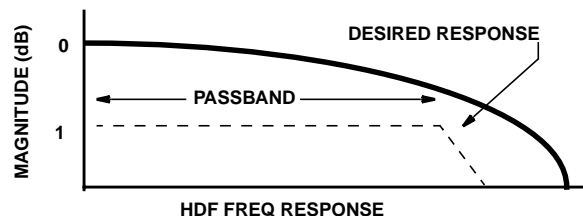
In Figure 1 the dotted line represents aliasing. The point defined by stopband attenuation (50dB) and the sum of the passband and transitionband frequencies, must not cross the dotted line. Sometimes in MANUAL design mode you will come upon a filter in which you can vary either the transitionband or passband frequencies or attenuation by just a few Hz or a few dB, and find the filter jumps from unrealizable due to many taps to a viable filter that only needs a few taps. This may be due to crossing the aliasing curve. This in effect, renders the HDF ineffective and DECIMATE is trying to accomplish everything in the FIR. You may also get the error message "HDF unrealizable".



**FIGURE 1.**

Violation of the second rule exhibits similar symptoms.

Figure 2 illustrates the design rule check that the HDF rolloff should not violate the passband attenuation spec. This condition can occur in a variety of ways, if the passband is a large percentage of the output rate; if the passband attenuation is very small; if most of the decimation is being done in the HDF (which brings the first null of the HDF response in close to the passband region). The number of stages in the HDF also determines the rolloff of the HDF response. This design rule check is done with no knowledge of the type of FIR being used, STANDARD, IMPORTED, or PRECOMP. Therefore, switching to a PRECOMP, or IMPORTED FIR will not alleviate a violation of this rule. The PRECOMP FIR can in fact, reduce the HDF rolloff effect when the rolloff is within the limits stated above.



**FIGURE 2.**

It is important the user understand which rule is being violated because the first one is hard and fast and must not be violated. The second is correctable with additional work (manual design of FIR on other software). It is of course possible that both rules are being broken. There are two simple tests that can be done to identify what the problem is. If the difficulty is with HDF rolloff in the passband (rule 2), then relaxing the passband attenuation will allow the software to generate a filter.

If the problem is intrusion of stopband attenuation past the dotted line (rule 1), then changing the passband attenuation will not solve anything. Try reducing the stopband attenuation, a little, then a lot, if this results in a filter design, then the problem is rule 1.

**Solutions**

If DECIMATE was in design mode MANUAL when the problem occurred, then the user can adjust the design parameters (input rate, output rate, passband, transition band, passband attenuation, stopband), or the HDF filter parameters to achieve a filter. For problems with rule 1 try any of the following: higher input rate, narrower passband, less stopband attenuation, less HDF decimation, more HDF stages. For problems with rule 2 try any of the following: higher input rate, higher output rate, narrower passband, looser passband attenuation, less HDF decimation, fewer HDF stages.

In general, if DECIMATE was in design mode AUTO when the problem occurred, then going to manual design mode and playing with HDF stages, or HDF decimation will not produce any better results (with the one exception noted below as "Special Case"). The user then must decide if the system can tolerate the relaxed design parameters (input rate, output rate, passband, transition band, passband attenuation, stopband attenuation) needed to achieve a realizable filter. If not, the user will need to perform a manual design of the HDF and FIR filter parameters.

**Special Case**

For those users who have the option of low system decimation rates there are some alternatives. For those with system decimation rates of less than 10, trying varying combinations of HDF decimation and HDF stages may prove worth while. Also, for those that can have system decimation of 16 or less, bypassing the HDF (setting HDF decimation to 1 and HDF stages to 0) and using only the FIR may be beneficial.

All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

*Intersil semiconductor products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.*

For information regarding Intersil Corporation and its products, see web site <http://www.intersil.com>

### **Sales Office Headquarters**

#### **NORTH AMERICA**

Intersil Corporation  
P. O. Box 883, Mail Stop 53-204  
Melbourne, FL 32902  
TEL: (321) 724-7000  
FAX: (321) 724-7240

#### **EUROPE**

Intersil SA  
Mercure Center  
100, Rue de la Fusee  
1130 Brussels, Belgium  
TEL: (32) 2.724.2111  
FAX: (32) 2.724.22.05

#### **ASIA**

Intersil (Taiwan) Ltd.  
7F-6, No. 101 Fu Hsing North Road  
Taipei, Taiwan  
Republic of China  
TEL: (886) 2 2716 9310  
FAX: (886) 2 2715 3029