

## Introduction

The Intersil HSP48908 2-D convolver has gained acceptance among customers as an excellent choice for implementing 8-bit 3x3 convolutional kernels. However, new applications in image processing, such as digital video broadcasting and medical imaging, demand higher bit resolutions. This technical brief shows how to implement a 3x3 10-bit kernel using the Intersil HSP43168 (Dual FIR Filter) and HSP9501 (Delay Buffer). This technique is also applicable, with appropriate modifications, to convolutions requiring greater than 10-bit resolution.

## 3x3 10-Bit Kernel

Figure 1 shows the block diagram of the 3x3 10-bit convolutional kernel. Use is made of two HSP43168s and two HSP9501s. This configuration will operate up to clock speeds of 32MHz.

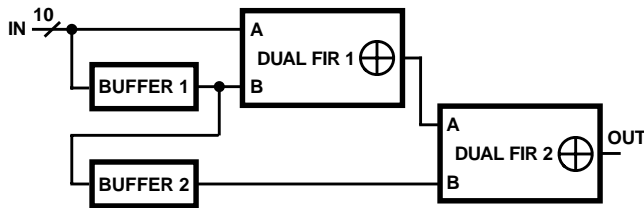


FIGURE 1. 1. BLOCK DIAGRAM OF 3x3 10-BIT CONVOLUTIONAL KERNEL

## Theory of Operation

A 3x3 convolution is implemented as the sum of three row vector dot products. Dual FIR 1 implements the top two row vector dot products and Dual FIR 2 implements the bottom row vector dot product. The convolution sum is facilitated via the A input of Dual FIR 2 and is available at the output of Dual FIR 2.

The row vector coefficients are programmed as the first 3 coefficients of Dual FIR 1 A and B and Dual FIR 2 B. The first coefficient of Dual FIR 2 A has a value of 1.0 with all other coefficients set to zero. Both dual FIRs have the output programmed to A + B (i.e. MUX1-0 is equal to 01).

Row buffer 1 is programmed for a length commensurate with the image row pixel length (e.g. 1024 pixels) while buffer 2 is programmed for the image row pixel length plus five additional delays. These five additional delays are needed to compensate for the pipeline delay associated with Dual FIR 1 (e.g. 1024 + 5 = 1029).

Because of the rounding feature in both dual FIRs, there is no need for shifting the MSB position at the output. The appropriate rounding value is programmed into control address 001H, bits 8-5, and is easily derived.

## Summary

A solution is presented for implementing a 3x3 10-bit convolutional kernel which makes use of two HSP43168 dual FIRs, programmed for A + B output, and two HSP9501 row buffers. Dual FIR 1 A and B, in conjunction with Dual FIR 2 B, implement the row vector dot products, while Dual FIR 2 A provides a path for summing the three dot products to obtain the convolution sum.

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