

Introduction

Optical Dual-in-line Flat No-lead (ODFN) packages are developed for light sensor applications. The mechanical structure of an ODFN is similar to that of a conventional DFN, except the molding compound is a transparent material rather than the conventional black compound. Transparent molding compound allows transmission of ambient light through the molding compound to reach the die sensor area. This package is Lead-free, with pre-plated Nickel-Palladium-Gold (NiPdAu) finish on the terminals. Figure 1 shows a 6 lead ODFN for illustration. As seen from the image, the package finish is transparent to allow light transmission and at the same time, protects the device from the environment.

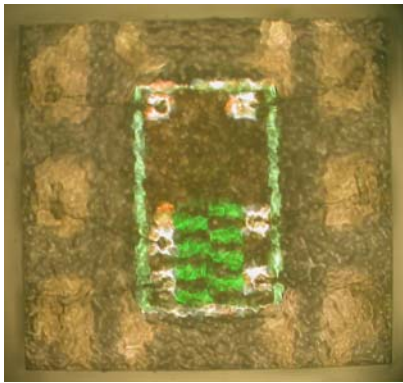


FIGURE 1. ODFN 6 LD PACKAGE TOP VIEW

This package follows conventional DFN/QFN guidelines for PCB land pattern design and surface mount processing. Some additional recommendations are made to accommodate the special clear mold compound, which has a lower glass transition temperature (Tg) and a higher coefficient of thermal expansion (CTE) compared to conventional molding compounds. This document provides guidelines for assembly and handling during board mount process.

Board Mounting Guidelines

The package board mounting process is similar to that of conventional DFN/QFN packages. However, there are some key differences in the materials used, therefore it is recommended that users account for these differences in their application method. Specific guidelines in this document are meant to accommodate for the differences in the materials.

Product Packing

ODFN products have been qualified under JEDEC MSL-3 test criteria, and are shipped in either a tube or tape-and-reel format. The packing quantity varies depending on the application and purchasing options. The moisture protection seal should not be broken until the board mounting process is ready. If the seal is broken, please follow standard instructions for baking per Jedec standard criteria for MSL-3 products.

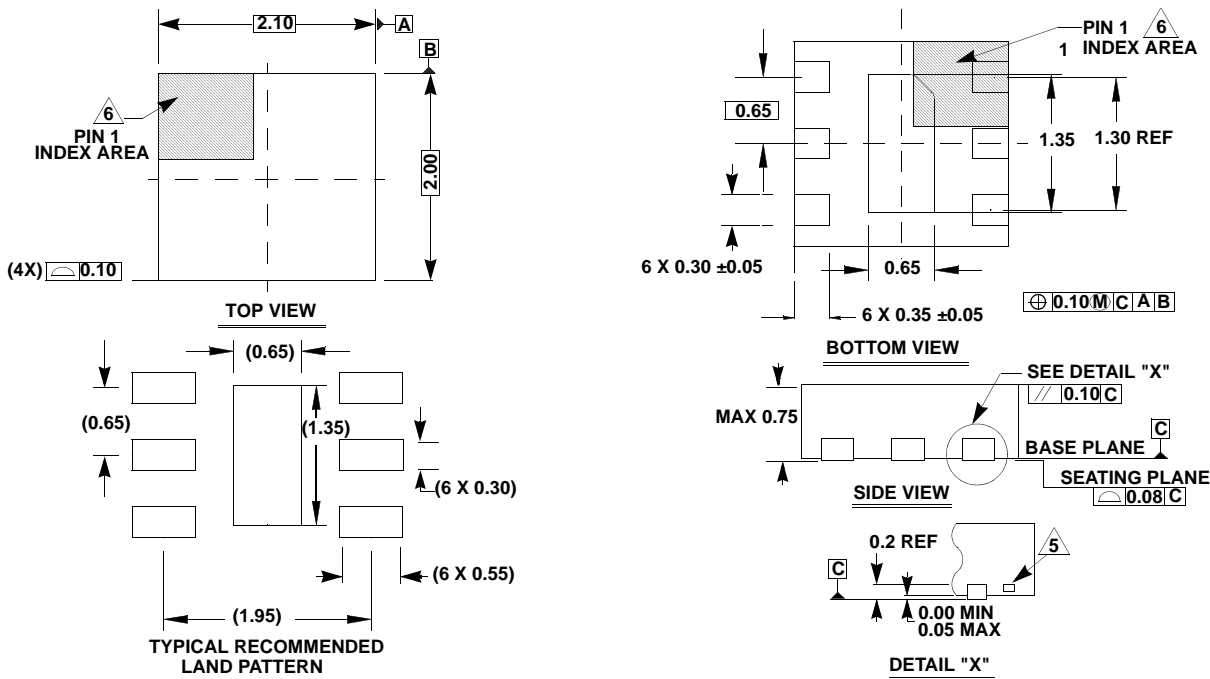


FIGURE 2. ODFN 6 LD PACKAGE DIMENSIONS

Package Construction

ODFN packages have a nominal package thickness of 0.7mm. Figure 2 shows a package outline drawing for the ODFN family with dimensions and tolerances. It is important to design PCB land patterns that correspond to the lead dimension as explained in subsequent section.

Similar to DFN and QFN packages, the ODFN has an exposed die paddle/pad as part of the package construction. As shown in Figure 2, the chamfered corner of the exposed thermal pad indicates Pin 1 location for the product. Similar to DFN or QFN, the exposed pad provides robustness to the overall solder joint strength after board mounting.

ODFN packages are assembled on pre-plated Copper lead-frames, and individual units are singulated by sawing process. The occasional presence of a slight oxide layer at the sawn surface of the Copper leads is not a concern for solder joint quality. Poor wetting to this exposed side edge does not impact the solder joint quality or reliability.

PCB Land Pattern Design

Intersil Technical Brief 389; (<http://www.intersil.com/design/packages/#TechBriefs>) provides detailed information for PCB design, DFN, QFN packages, and is applicable to ODFN packages. Additionally, package specific land pattern information is available on package outline drawings which are located on the following website: <http://www.intersil.com/design/packages/>. The package outline drawings are also included in product datasheets. An

example of land pattern recommendation is shown in Figure 3 (ODFN 6L). The main features can be summarized as follows:

- 1:1 match with exposed pad area (In case of ODFN 6L, 0.65mm x 1.35mm)
- 1:1 match with pin width (In case of ODFN 6L, 0.3mm)
- Land length for pin = pin length + 0.2mm (extending out from the package edge)

Figure 4 shows a reference solder joint shape after ODFN package mounting on PCB. Solder joint under the exposed pad is intended to provide the package stand-off height and robust assembly

The pad definition on the board is recommended to be non-solder-mask-defined (NSMD), though solder-mask-defined (SMD) pads of the same effective wettable dimension are acceptable as well. A Nickel/Gold surface finish with 0.2 micron maximum gold thicknesses is recommended for good solder wettability and shelf-life for the SMT process. OSP surface finish is also acceptable, but requires appropriate controls on shelf life and exposure of PCB to environment. HASL or solder plated finishes (pre-plated solder) should not be used for these products.

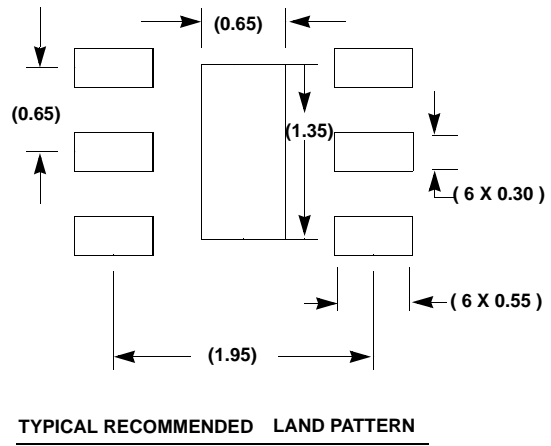
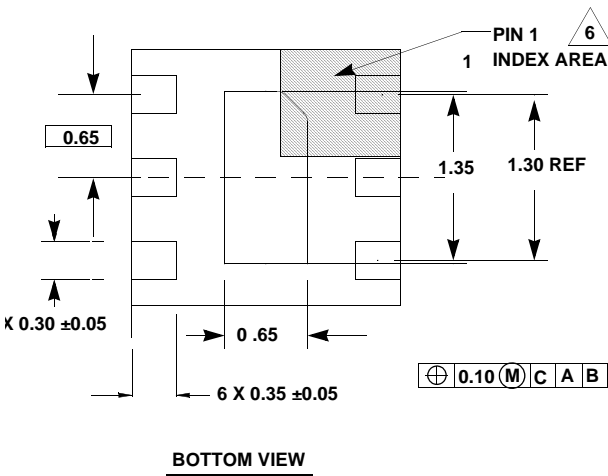


FIGURE 3. ODFN 6 LD FOOTPRINT (LEFT) AND CORRESPONDING LAND PATTERN FOR PCB DESIGN (RIGHT)

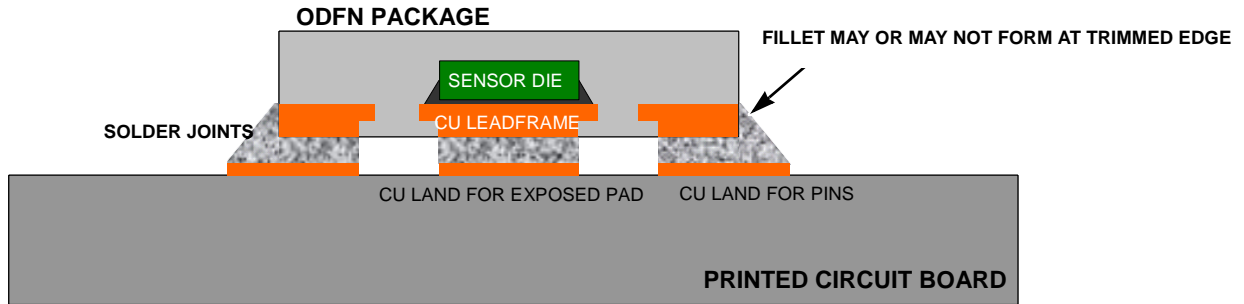


FIGURE 4. SCHEMATIC SHOWING ODFN PACKAGE MOUNTED ON PCB

Solder Stencil

- 0.100mm or 0.125mm thick stainless steel stencil is recommended.
- The stencil should be laser-cut followed by electro-polish (chemical finishing not recommended). Alternatively an additive build-up stencil may be used.
- Solder Paste volume is a key contributor to solder joint reliability (higher solder volume leads to greater reliability). However, this needs to be controlled, as solder bridging may occur when the solder paste is excessive.
- It is highly recommended to solder the exposed package pad to the corresponding landing pad on the PCB. Care should be taken to ensure there is no excessive solder under the exposed area, as this can cause open solder joints due to excess stand-off created by the exposed pad. The optimal value for solder paste in center pad is 70% to 80% solder paste coverage on the exposed pad area.

Solder Paste

The package itself is lead-free, and is compatible with both eutectic Tin/Lead or lead-free Tin/Silver/Copper solders. These packages have been qualified at a +235 °C maximum temperature reflow profile for eutectic solder, and at a +260 °C maximum temperature reflow profile for lead-free solder. Solder paste with “no-clean” flux and “Type 3” or “Type 4” solder particle size distribution is recommended.

Reflow Profile

Direct infrared (IR) heating of these packages must not be done as it can damage the part. Pure convection reflow of these parts is recommended. Typical reflow profiles per Jedec J-STD-020 criteria are recommended for the eutectic Sn/Pb and Lead-free Sn/Ag/Cu solders. Peak temperature for the eutectic Sn/Pb profile is not to exceed +235 °C. The Lead-free profile is not to exceed +260 °C.

Visual Inspection

Visual inspection of solder joints should be done to verify that there is no solder bridging between pads, and that the solder joint is “bright-and-shiny” (lead-free appears ‘dull’ compared to Sn/Pb). The package is not to be tilted or

off-center with respect to the PCB land pattern. A solder fillet at the edge of the package leads is not a requirement, and in fact may not form at all. Hand solder touch-up is not recommended as excess heat from the air nozzle or soldering iron can damage the transparent mold compound.

ODFN Specific Application Guidelines

The transparency requirement of Ambient Light Sensing products (ALS) does not allow conventional filler loading as a means for controlling mechanical properties of the mold compound (such as coefficient of thermal expansion (CTE), modulus, glass transition temperature (T_g)). As such, the CTE of a clear epoxy is higher than a conventional black epoxy with fillers, has a lower modulus, and a lower T_g. The following sections outline features of the ODFN product for proper application of the product.

Sensor Location and Optics Design

In general, the package body center does not always coincide with the center of the light sensor. The sensor location (green area in top part of IC) is offset from the geometric center of the IC. The location of the sensor itself is specific to the product design in question, and therefore should be obtained from the product datasheet. Figure 5 shows an example of the sensor location description. In this example, the sensor area is 0.43mmx0.61mm, and it is offset from the center of the IC by 0.25mm. The application set-up should be designed to lead the light to the center of the sensor area and not to the center of the package. On the other hand, the sensor surface height is always located at 0.28 ±0.10mm below the top surface of the package. Solder joint and package height (0.7mm) should also be considered in calculating the sensor surface height from the PCB top surface.

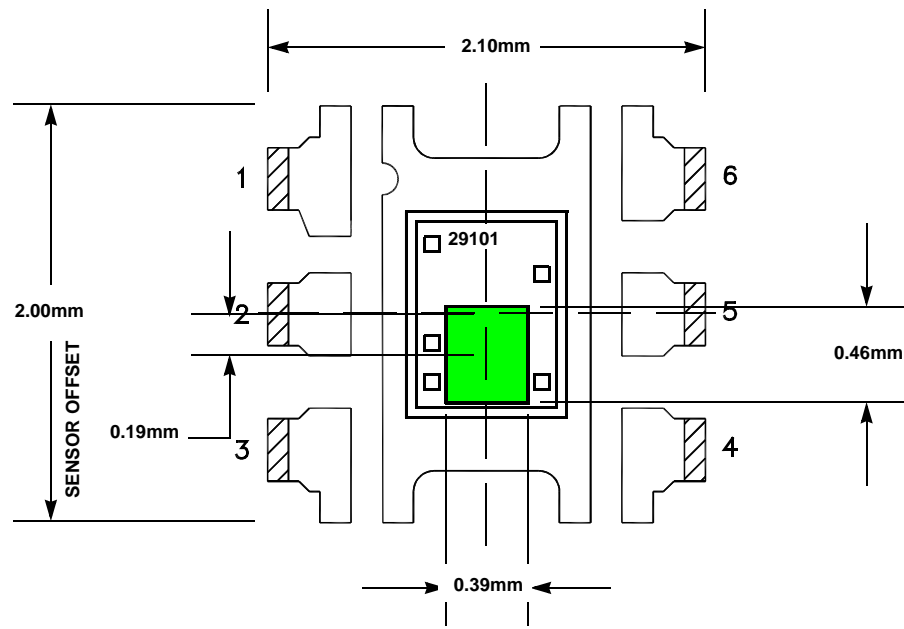


FIGURE 5. EXAMPLE OF SENSOR LOCATION DESCRIPTION

Moisture Sensitivity and Bake Conditions

ODFN packages have been qualified at JEDEC moisture sensitivity levels of MSL3 for both +235°C and +260°C solder reflow profiles. The properties of clear mold compound are such that moisture saturation occurs rapidly. Therefore, it is important to control the exposure time once the moisture protection seal is broken. It is recommended that ODFN components be baked according to the moisture sensitivity level labeling on the reel if the exposure time exceeds the recommended level on the label prior to board mounting.

The recommended baking condition is +100°C for 24 hours. A bake temperature higher than +100°C can result in discoloration of the clear molding compound.

Pick-And-Place With Clear Packages

These optically clear packages are fully compatible with vision-based placement machines. These packages are not recommended to be placed with mechanical centering placement machines or Chip-shooters.

Rework and Associated Risks

ODFN products can be reworked using a reflow profile that closely matches the production reflow profile described earlier. ODFN packages should not be exposed to >260°C during rework operation. Do not reuse the same ODFN product upon removal from the PCB. Replacement unit should be used. Excessive heating of clear mold compound can result in change in color of the mold compound and can also compromise wire bond integrity due to high coefficient of thermal expansion of the mold compound material.

Marking and Traceability

ODFN products cannot be marked on the top side of the package due to the need for unobstructed transparency. On the bottom of the package, there is a 4-letter code laser-marking that can be used to trace the lot and part details. In addition, in viewing from the top, the lead-frame has a special pin 1 notch cut-out in the exposed pad next to the pin 1 lead. This allows checking of the correct pin 1 orientation after mounting on the PCB.

Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that the Application Note or Technical Brief is current before proceeding.